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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,865	10/30/2003	Andreas C. Doering	RPS920030110US1	8071

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EXAMINER	
CODY, DILLON J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,865	DOERING ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *30 October 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and information disclosure statement, all filed 30 October 2003 and disclosure filed 4 March 2004.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by De Oliveira Kastrup Pereira et al. (U.S. Patent No. 6,721,884) hereinafter referred to as Pereira.

6. As per claim 1, Pereira discloses a method for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor (Fig. 1 reconfigurable logic 18 and col. 1 lines 28-29), the coprocessor coupled to a processor (Fig. 1), the method comprising:

(a) beginning an execution of an application by the processor; (Col. 4 lines 54-57)

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application; (Col. 5 lines 45-49)

(c) determining that the FPGA in the coprocessor is not programmed with logic for the function; (Col. 5 lines 53-59)

(d) fetching a configuration bit stream for the function; (Col. 5 lines 53-59)

(e) programming the FPGA with the configuration bit stream. (Col. 5 lines 53-59)

7. As per claim 2, Pereira discloses the method of claim 1, wherein the issuing step (b) comprises:

(b1) receiving the instruction by an Auxiliary Processing Unit (APU) interface (Fig. 2 control circuit 23) between the processor and the coprocessor.

8. As per claim 3, Pereira discloses the method of claim 2, wherein the determining step (c) comprises:

(c1) determining that the APU interface issued a faulty commit. (Col. 5 lines 53-59)

9. As per claim 4, Pereira discloses the method of claim 1, wherein the fetching step (d) comprises:

(d1) initiating an exception subroutine by the processor; and (Col. 6 lines 1-3)

(d2) fetching the configuration bit stream for the function by an exception subroutine of the processor. (Col. 6 lines 1-3) *The examiner asserts that "stalling the processor" and processing a separate task (loading the new configuration file) constitutes executing an exception subroutine.*

10. As per claim 5, Pereira discloses the method of claim 4, wherein the initiating step (d1) comprises:

(d1i) determining that the coprocessor issued a faulty commit; (Col. 5 lines 53-59) and

(d1ii) branching to the exception subroutine by the processor in response to the faulty commit. (Col. 6 lines 1-3) *The examiner asserts that Pereira's processor inherently branches to the subroutine for loading the new configuration file if the subroutine is to be executed.*

11. As per claim 6, Pereira discloses the method of claim 4, wherein the fetching step (d2) comprises:

(d2i) decoding a function identifier by the exception subroutine; *The examiner asserts that a function must inherently be identified to the subroutine if the correct configuration file is to be fetched and loaded.*

(d2ii) requesting and being granted ownership of the function; *The examiner asserts that if the processor loads the new configuration file to perform a function it must inherently have ownership of the function-performing configuration file.*

(d2iii) fetching the configuration bit stream for the function from a memory; (Col. 5 lines 53-57)

(d2iv) identifying an exception type and a coprocessor instruction type for the configuration bit stream; *The examiner asserts that the processor must inherently identify the exception request thrown by the control circuit 23 if it is to run the proper subroutine and load the proper configuration file.*

(d2v) sending the configuration bit stream to the coprocessor. (Col. 5 lines 53-57)

12. As per claim 7, Pereira discloses the method of claim 1, wherein the programming step (e) comprises:

(e1) performing a sequence of load and store instructions by an exception subroutine of the processor to program the FPGA with the configuration bit stream. *The examiner asserts that with a limited number of bit-lines dedicated to programming the FPGA (Fig. 2 ports 20a,b and 22) and the "considerable overhead" required for loading a configuration file (Col. 2 lines 6-7), Pereira's*

processor must inherently perform multiple store instructions to transfer the data of the configuration file into the reconfigurable logic.

13. As per claim 8, Pereira discloses the method of claim 1, further comprising:

(f) receiving a reissuance of the instruction by the coprocessor. *The examiner asserts that after the reconfigurable logic has been reconfigured, the instruction is re-issued to the newly configured logic. (Col. 5 lines 59-60)*

14. As per claim 9, Pereira discloses a method for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor (Fig. 1 reconfigurable logic 18 and col. 1 lines 28-29), the coprocessor coupled to a processor, the method comprising:

(a) beginning an execution of an application by the processor; (Col. 4 lines 54-57)

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application; (Col. 5 lines 45-49)

(c) issuing a faulty commit when the FPGA in the coprocessor is not programmed with logic for the function; (Col. 5 lines 53-59)

(d) initiating an exception subroutine by the processor in response to the faulty commit; (Col. 6 lines 1-3)

(e) fetching a configuration bit stream for the function by the exception subroutine; (Col. 6 lines 1-3) *The examiner asserts that "stalling the processor"*

and processing a separate task (loading the new configuration file) constitutes executing an exception subroutine.

(f) performing a sequence of load and store instructions by the exception subroutine to program the FPGA with the configuration bit stream. *The examiner asserts that with a limited number of bit-lines dedicated to programming the FPGA (Fig. 2 ports 20a,b and 22) and the "considerable overhead" required for loading a configuration file (Col. 2 lines 6-7), Pereira's processor must inherently perform multiple store instructions to transfer the data of the configuration file into the reconfigurable logic.*

15. As per claim 10, Pereira has taught a computer readable medium including instructions performing the method of claim 1, consequently claim 10 is rejected for the same reasons set forth in the rejection of claim 1 above.

16. As per claim 11, Pereira has taught a computer readable medium including instructions performing the method of claim 2, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

17. As per claim 12, Pereira has taught a computer readable medium including instructions performing the method of claim 3, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

18. As per claim 13, Pereira has taught a computer readable medium including instructions performing the method of claim 4, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

19. As per claim 14, Pereira has taught a computer readable medium including instructions performing the method of claim 5, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

20. As per claim 15, Pereira has taught a computer readable medium including instructions performing the method of claim 6, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

21. As per claim 16, Pereira has taught a computer readable medium including instructions performing the method of claim 7, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 7 above.

22. As per claim 17, Pereira has taught a computer readable medium including instructions performing the method of claim 8, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

23. As per claim 18, Pereira has taught a computer readable medium including instructions performing the method of claim 9, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

24. As per claim 19, Pereira discloses a system, comprising:

a processor for executing an application; (Fig. 1)

a coprocessor coupled to the processor, the coprocessor comprising Field Programmable Gate Arrays (FPGA); (Fig. 1 reconfigurable logic 18 and col. 1 lines 28-29)

and a memory coupled to the processor and the coprocessor, the memory comprising at least one configuration bit stream for a function, (col. 5 lines 53-57)

wherein an instruction is issued to the coprocessor by the processor to perform the function for the application during execution of the application, (col. 5 lines 7-12)

wherein the coprocessor determines that the FPGA is not programmed with logic for the function, (Col. 5 lines 53-57)

wherein the at least one configuration bit stream for the function is fetched, wherein the FPGA is programmed with the at least one configuration bit stream. (Col. 5 lines 53-57)

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hastie et al. (Hastie, N; Cliff, R. "The Implementation of Hardware Subroutines on Field Programmable Gate Arrays." Proceedings of the IEEE. IEEE 1990 Custom Integrated Circuits Conference. 13-16 May

1990. Pages 31.4.1-4) disclose a processor replacing configurations on an FPGA coupled to a processor.

Casselman (U.S. Patent No. 6,023,755) discloses a system allowing replacement of portions of an FPGA's configuration in real-time processing.

26. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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